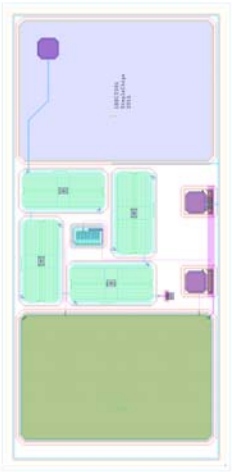
- Maximum Voltage. . . 1500 V
- Nominal Ratio = 0.000735
- Mask Programmable Ratio from 1.0E-5 to 0.200
- Integrated Low-Pass Filter (RC=38uSec nominal)
- High Nominal Resistance 80Meg

DIE

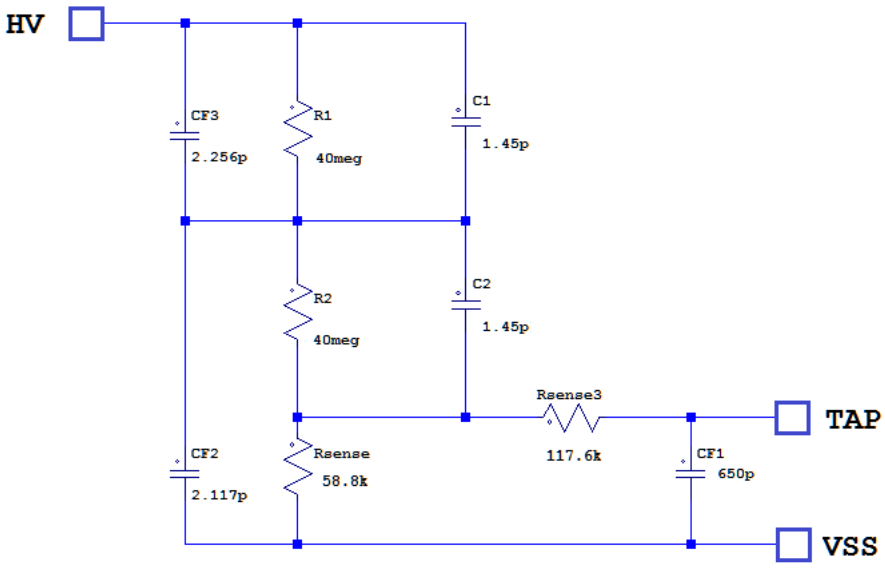
(TOP VIEW)



Description

This device is a high-voltage (1.5KV) voltage divider typically used in systems requiring the ability to sense high voltages for example those generated from an embedded charge-pump. The chip has a built-in low-pass filter allowing the chip to filter voltage changes typical of voltage pumping frequencies while allowing accurate voltage measurements when the pump is turned-off. The voltage divider ratio is mask programmable in a wide range from 1.0E-5 to 0.2000.

Equivalentcircuit:



Absolute maximum rating

Input Voltage (V_{HV} - V_{SS}) . . . . . +/-1500 V
Output Voltage . . . . . -0.6/+20V
Operating temperature . . . . . -40 C to 100 C
Storage temperature. . . . . -65 C to 125 C

Recommended operating conditions

PARAMETER	MIN	MAX	UNIT
Operating voltage (V_{HV} - V_{SS})	0	1500	V

DC Electrical charateristics at room temperature (RT = 25C +/- 5C)

PARAMETER		TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNIT
R_{sense0}	Divider Ratio	V_{HV}=+100V	RT	700	735	770	µV/V
R_{sense1}	Divider Ratio	V_{HV}=+500V	RT	700	735	770	µV/V
R_{sense2}	Divider Ratio	V_{HV}=+1500V	RT	700	735	770	µV/V
R_{TOT}	Total Resistance	V_{HV}=+500V	RT	40.0	80.0	120.0	MegΩ
R_{Sense}	Sense Resistor	V_{TAP}=1.00V; V_{HV}=0V	RT	28.0	58.8	92.4	kΩ
ΔR/R	Resistor Divider Linearity	R@100V; R@1500V (3 seconds duration)	RT	-0.00	+0.35	+1.5	%
T_{C1}	Resistance First Order Temperature Coefficient	T -40C to 85C	-		-4400		ppm/C
T_{C2}	Resistance Second Order Temperature Coefficient	T -40C to 85C	-		+12.2		ppm/C^2
C_{F1}	Filter Capacitance	I=10nA	-		650		pF

AC Operating charateristics (RT = 25C +/- 5C)

PARAMETER		TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNIT
T_{SET}	Filter Setlling Time (95% of DC value)	V_{HV}=0V -> 50V	RT	100	250	1000	µSec

TYPICAL CHARACTERISTICS

Die dimensions

PARAMETER		MIN	TYP	MAX	UNIT
Y_{SIZE}	Long Side Dimensions	2250	2350	2450	µm
X_{SIZE}	Short Side Dimensions	1050	1150	1250	µm
Z_{SIZE}	Die Thickness	260	285	310	µm

Visual inspection

PARAMETER	Lot Sampled	Sample Size	Fails Allowed	UNIT
100% Visual Inspection per MIL STD 883H Method 2010 Condition B.	ALL	100%	n/a	n/a

Product qualification tests

PARAMETER	Lot Sampled	Sample Size	Fails Allowed	UNIT
Static burn-in 504hrs @ V_{HV}=1000V; MIL STD 883 method 1015	3	22	0	n/a
Physical dimensions	3	11	0	n/a
Wire Bond Evaluation (Gold Ball Bond) per MIL STD 883 method 2011	3	20	1	n/a

Lot acceptance tests

PARAMETER	Lot Sampled	Sample Size	Fails Allowed	UNIT
Static burn-in 168hrs @ V_{HV}=1000V; MIL STD 883 method 1015	each	22	0	n/a
Physical dimensions	each	11	0	n/a
Wire Bond Evaluation (Gold Ball Bond) per MIL STD 883 method 2011	each	20	1	n/a

Product qualification tests are done on 3 batches only while lot acceptance test are performed on each “diffusion lot”. Lot acceptance tests (LAT) are considered done if the lot in question was used for product qualification.

All samples used for qualification and LAT burn-in test are assembled in a open cavity ceramic DIL package with a dielectric silicone gel filling the cavity where the chip is mounted to provide isolation between the wirebonds and the substrate and to eliminate surface conduction and polarization as possible means of unwanted failure.

Application note

To make best use of the 18SCT001 the chip should be molded before high voltage is applied to it. This can either be done with a standard mold compound or with silicone gel. Care should be taken when selecting a encapsulant to ensure proper dielectric strength and of course resistance. We recommend that the dielectric strength of the dielectric used be greater than 10kV/mm at a thickness of 50um.

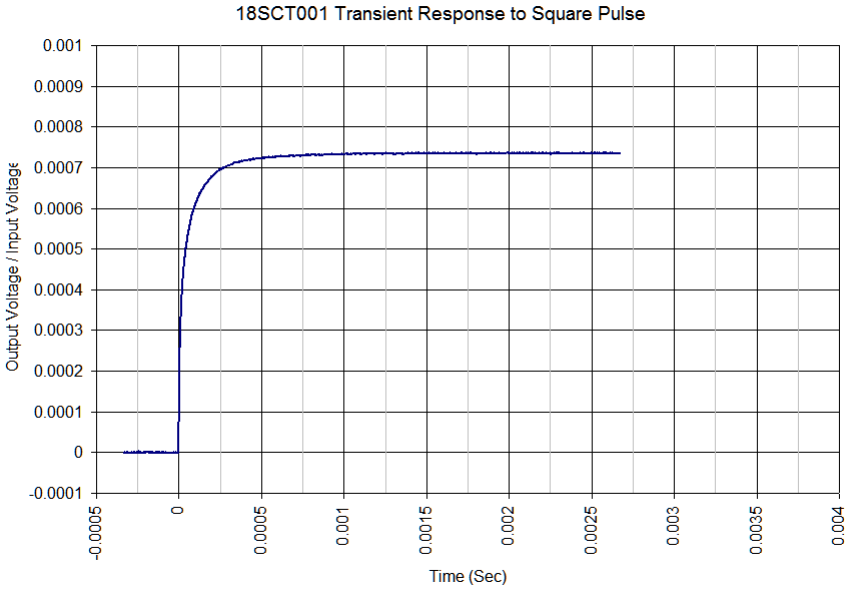
Care should also be taken to properly isolate the chips substrate which is biased at about half V_{HV}. In no circumstance should the chip be mounted over layers providing less than 2kV of dielectric isolation.Itis also strongly recommended to use non-conducting epoxy for attaching the chip.

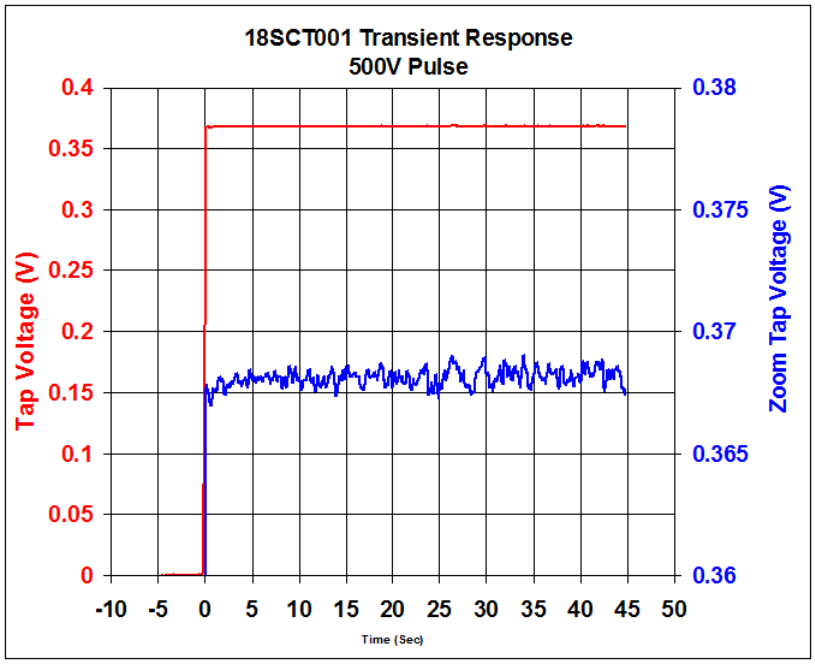
Low capacitance between the substrate node and Vss or HV is also important. There is an internal capacitor (see Equivalent circuit on page 1) of about 2pF in value between these node and any additional capacitance will increase the 18SCT000’s time constant.

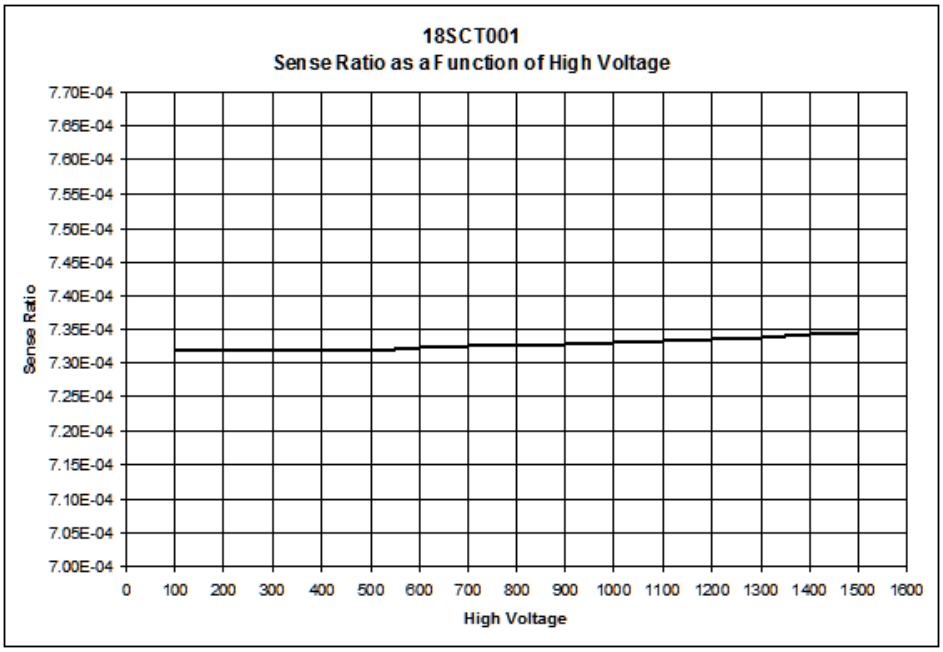
It is recommended that the chip be mounted with non-conducting epoxy (25um thickness+) over an area free of underlying conductors over a thickness of at least 100um.

Ball bonding should be used for attaching conductors to the chip’s pad. Wedge bonding is not recommended because of the shorter distance between the wirebond and the chip’s edge increasing the risk of arcing/shorting under high voltage. When using ball bonding the wire should extend vertically for at least 100um before going horizontal toward the substrate of package pad.

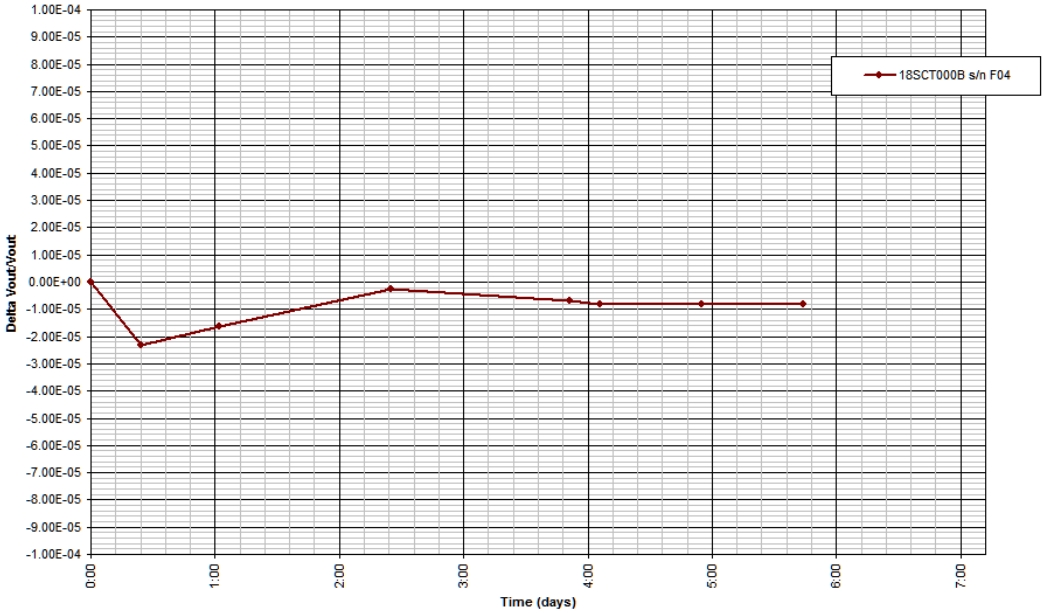
Dividing Ratio Transient Response (Typical)







Drift at 1kV (room temp)



DIMENSIONS