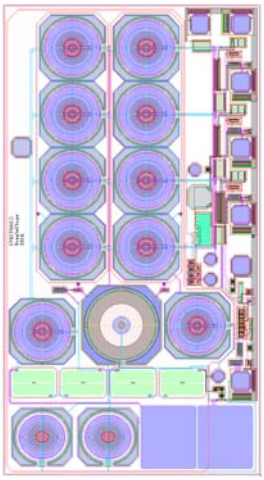
17SCT002
DIRECT-COUPLED HIGH-VOLTAGE (1kV) CURRENT LIMITER

17SCT002 - PRELIMINARY SPECIFICATION - REVISION JUNE 3, 2017

- Maximum Voltage. . . 1,100 V
- Zero External Components
- HV Current Sink Enabled by Direct-Coupled LV Control
- HV Sink Current Limited, independent of HV
- Low HV Idle Current

DIE
(TOP VIEW)



Description

The 17SCT002 is direct coupled high voltage current limiter chip. When the enable signal is asserted, the high-voltage (HV) terminal will sink a current that is limited and independent of HV (above a knee voltage). Upon deassertion of the enable signal, the 17CT002 presents a high resistance to the HV terminal.

Absolute maximum ratings

Input High Voltage (HV_{dd} - LV_{ss}) . . . . . 1100 V
Input Low Voltage Enable (V_{enable} - LV_{ss}) . . . . . 20 V
Storage temperature. . . . . -65 C to 150 C

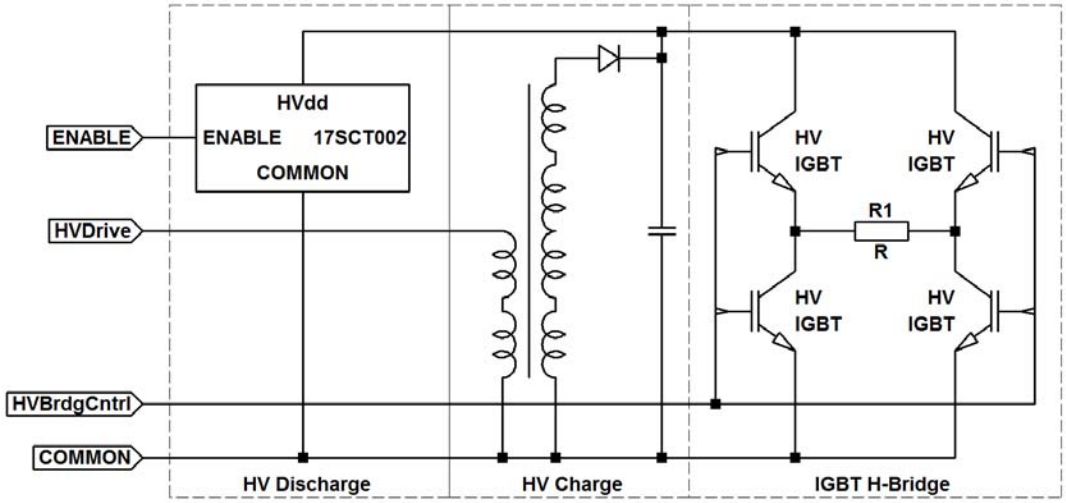
Recommended operating conditions

PARAMETER	MIN	MAX	UNIT
Operating Voltage (HV_{dd} - LV_{ss})		1000	V
Operating Voltage (Enable)	6	17	V
Operating Temperature	-40	150	^{o}C

Pin definitions

SYMBOL	DESCRIPTION
HV_{dd}	High-Voltage Terminal; 0 - 1000V
LV_{ss}	Common Terminal; 0V
Enable	Enable

Typical application

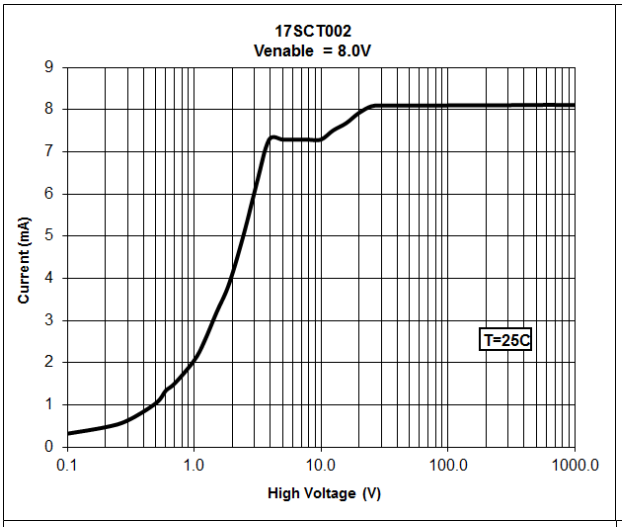


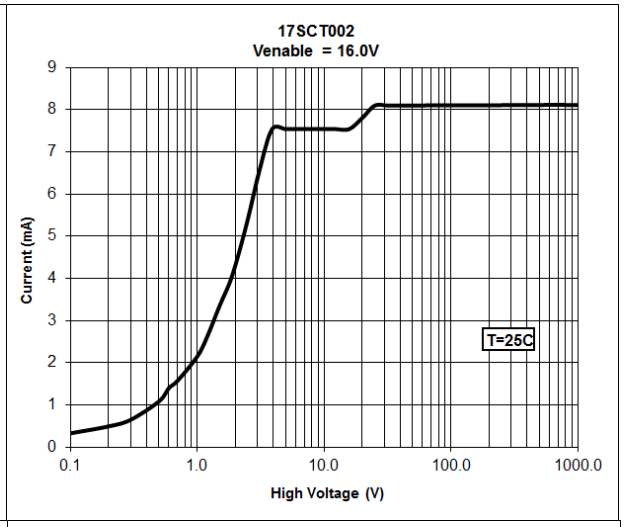
Static electrical characteristics(25C ± 2°C)

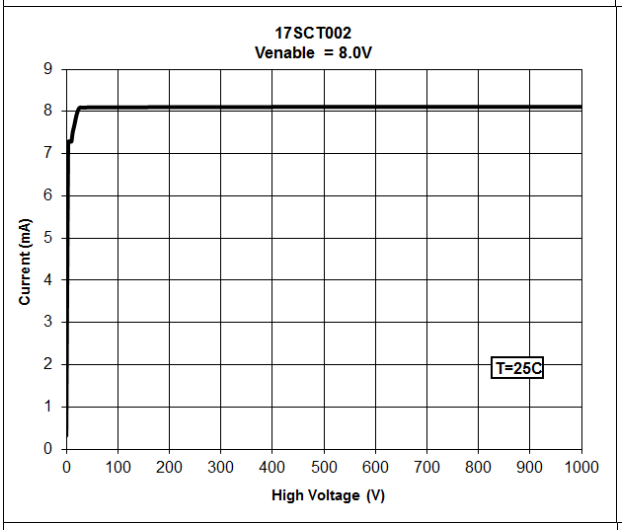
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HV_{ddmax}	Maximum High Voltage	i_{HVdd}=50μA, Enable=0V	1000	1100	N/A	V
I_{HVdd30}	Current Limit	HV_{dd}=30V, Enable=8V	7.6	8	8.4	mA
I_{HV1}	HV_{dd} current at 1V	HV_{dd}=1V, Enable=8V	1.3	2.3	3.5	mA
VE_{max}	Maximum Enable Voltage	HV_{dd}=0V, I_{Enable}=1mA	20	23	N/A	V
$I_{HVddmax}$	Maximum Leakage Current	HV_{dd}=1000V, Enable=0V	7	13	25	μA
$Delta_{HVddmax}$	Maximum i_{HVdd} Variation	I(HV=1000V)-I(HV=30V) @ Enable=8V	-0.1	0	0.1	mA
I_{E8V}	Maximum Enable Current at 8V	HV_{dd}=0V, Enable=8V	0.1	0.21	0.3	mA
I_{E16V}	Maximum Enable Current at 16V	HV_{dd}=0V, Enable=16V	0.3	0.47	0.65	mA
$V_{EIHVdd30gt7}$	Enable Voltage for I>7mA	HV_{dd}=30V, sweep Enable to IHV_{dd}>=7mA	0.6	1	2	V
$V_{EIHVdd5gt5}$	Enable Voltage for I>5mA	HV_{dd}=5V, sweep Enable to IHV_{dd}>=5mA	3.5	4.7	6	V

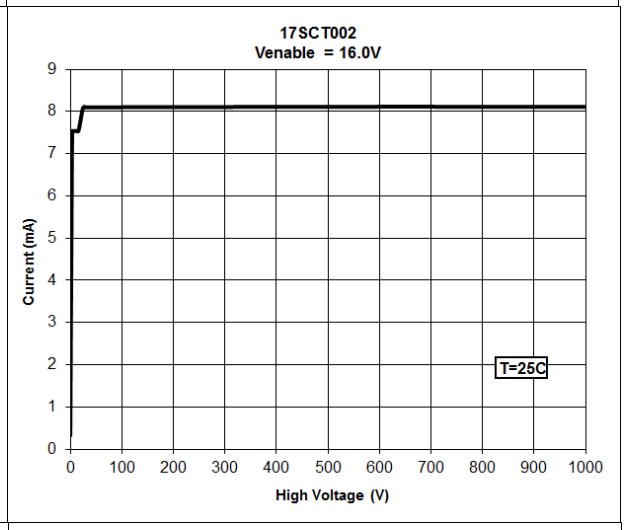
Dynamic electrical characteristics (25°C ± 2°C)

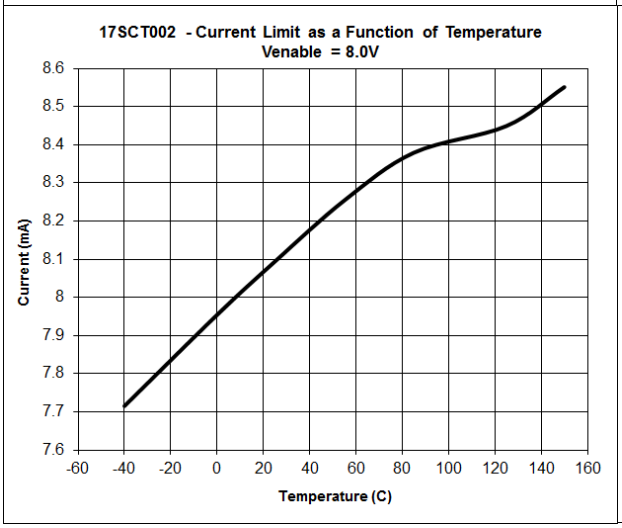
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ond}	Turn-on Delay to 1mA	HV_{dd}=30V, Enable=0 to 8V	0.4	0.8	1.5	μS
t_r	Rise time from 1mA to 7mA	HV_{dd}=30V, Enable=0 to 8V	0	0.1	0.5	μS
t_{offd}	Turn-off delay to 7mA	HV_{dd}=30V, Enable=8 to 0V	0	0.1	0.5	μS
t_f	Fall time from 7mA to 1mA	HV_{dd}=30V, Enable=8 to 0V	2	4	6	μS

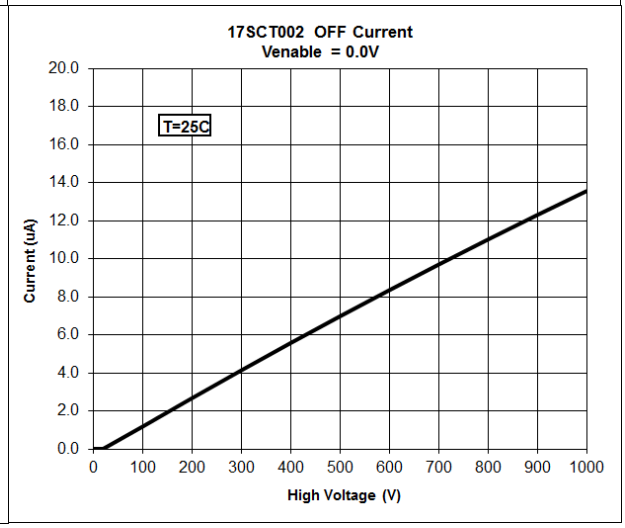


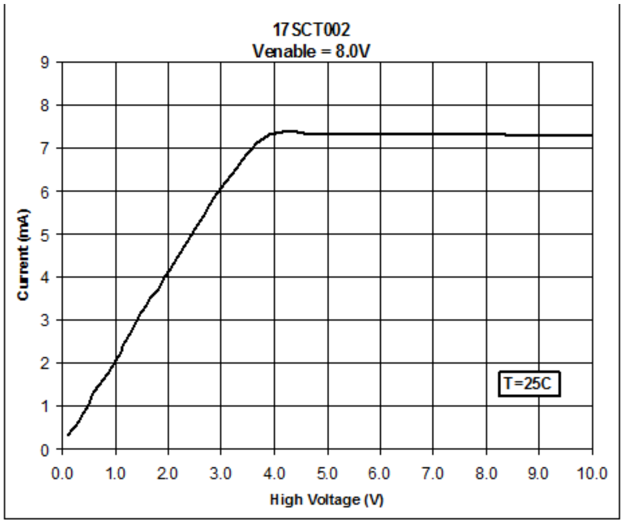


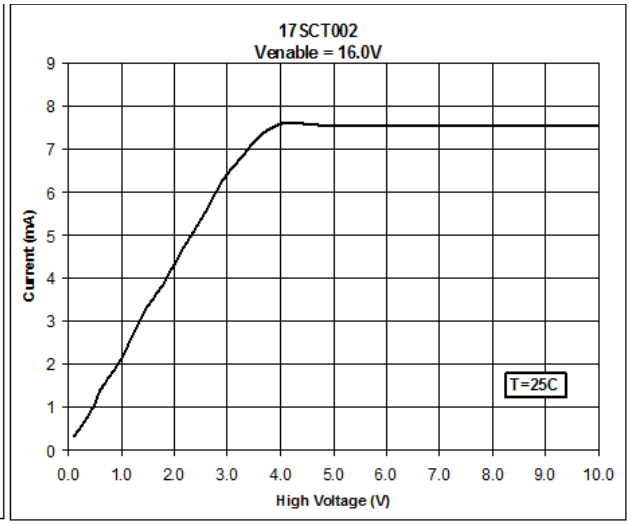


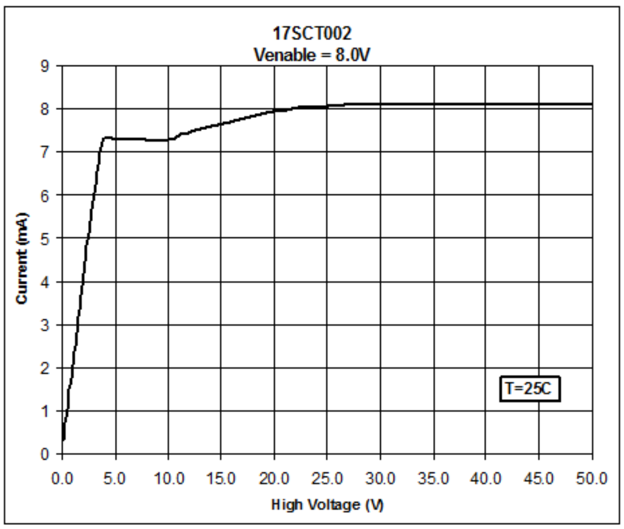


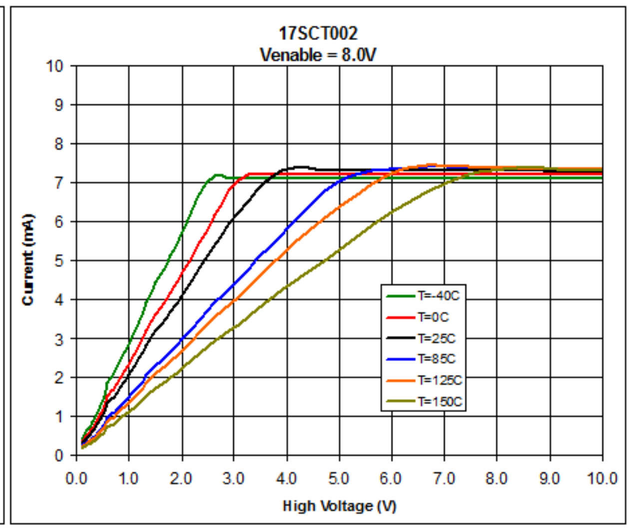


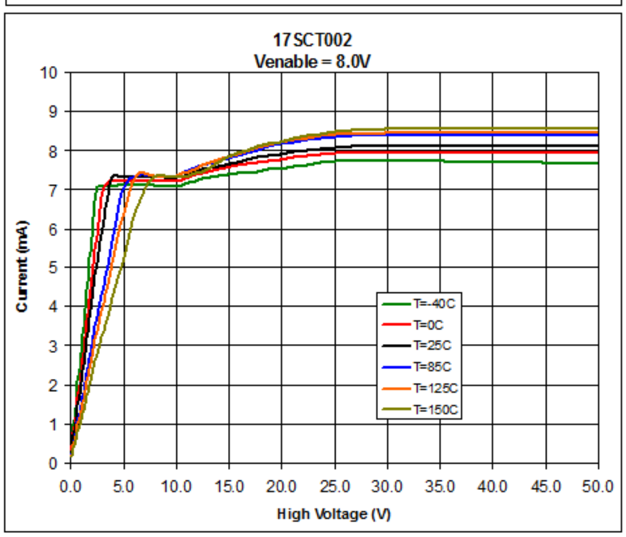


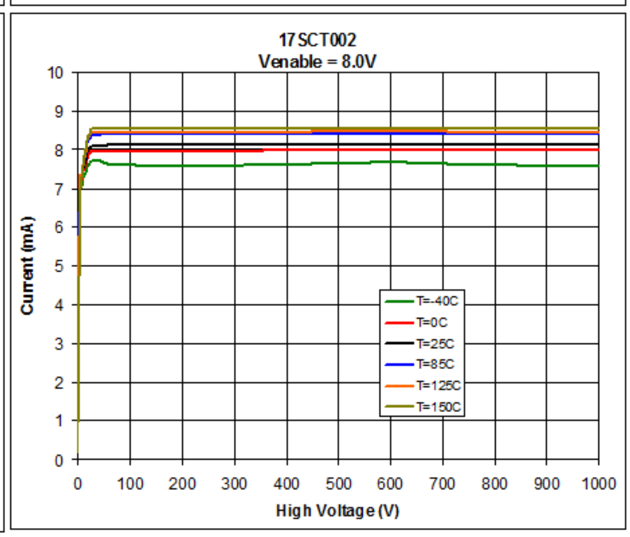


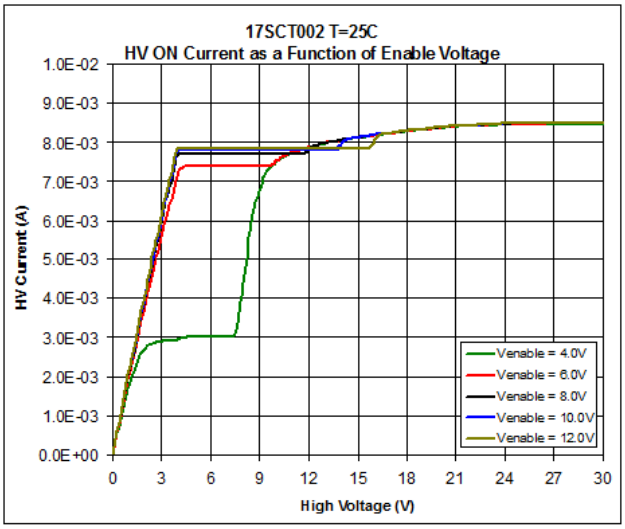


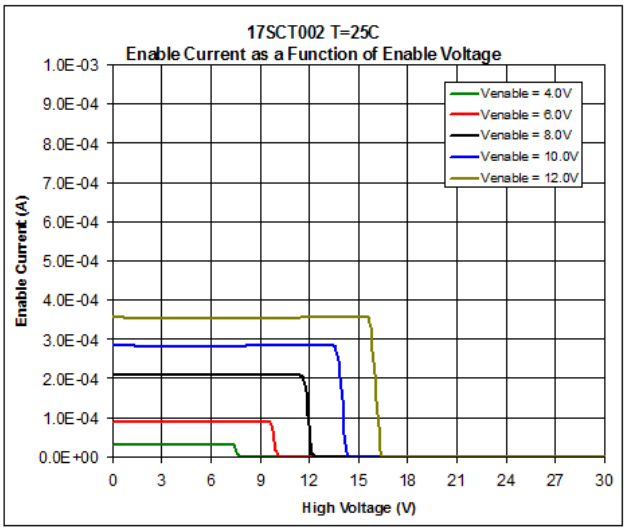


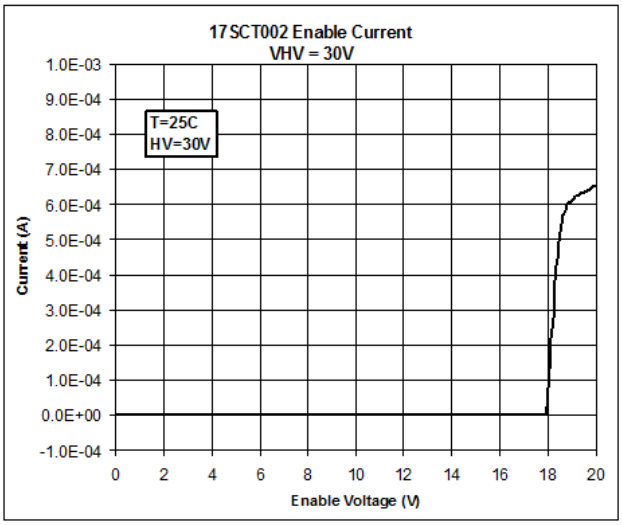


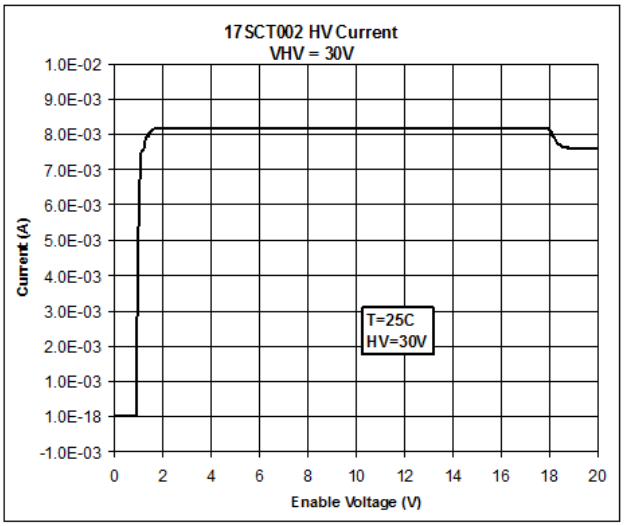


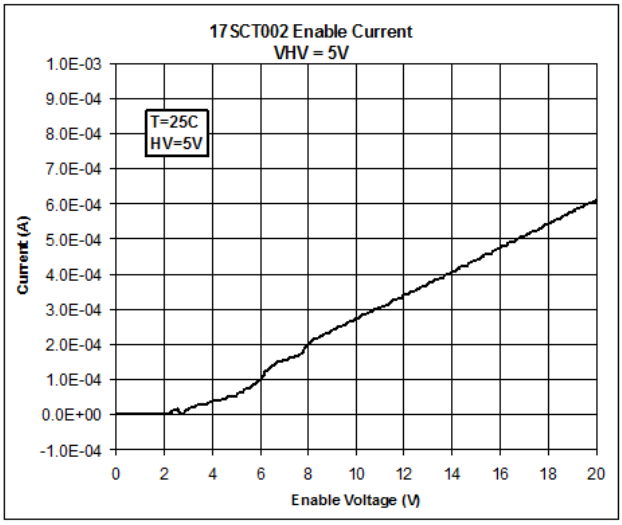


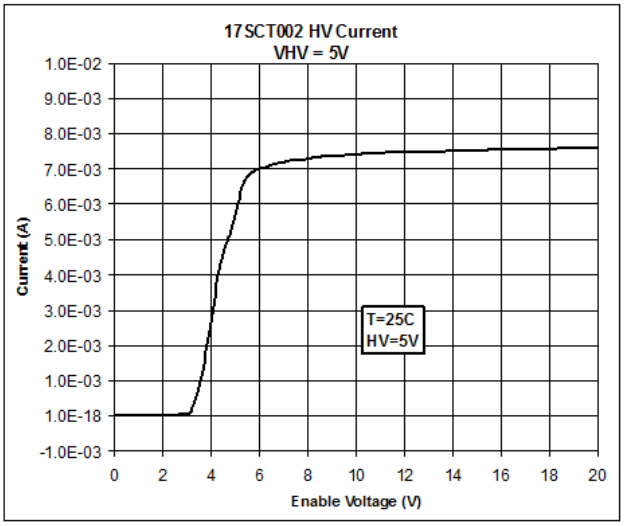


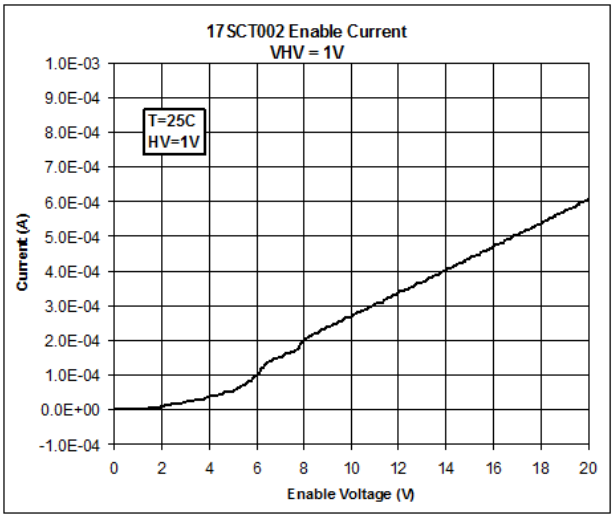


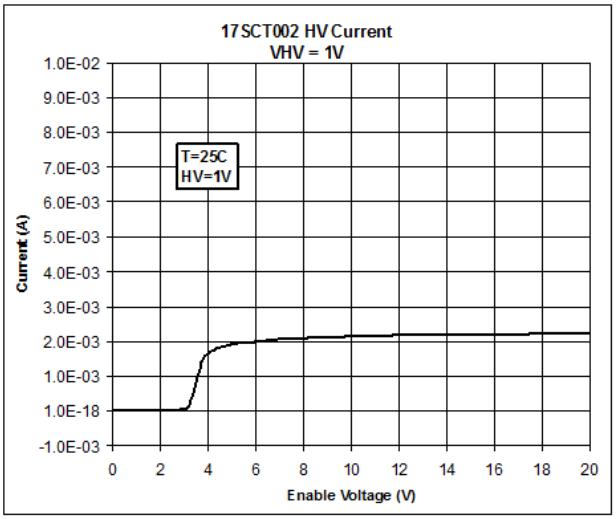


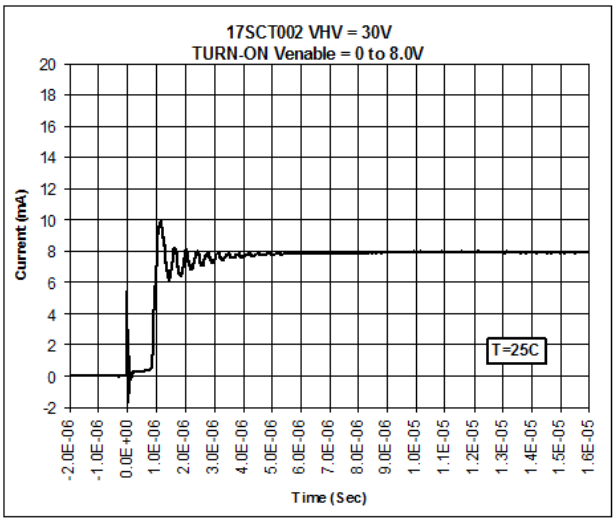


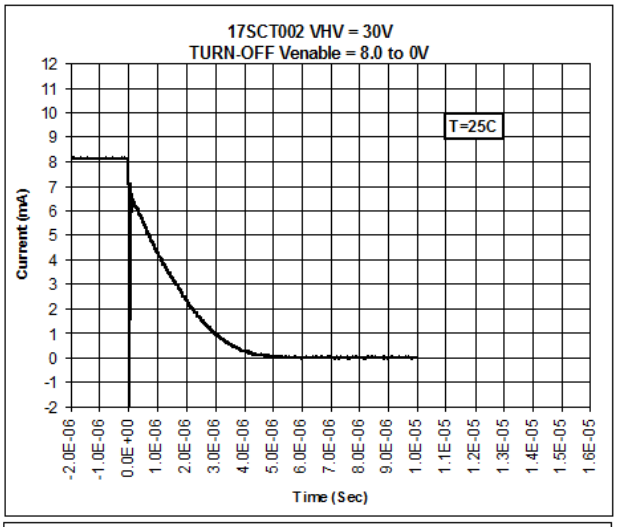


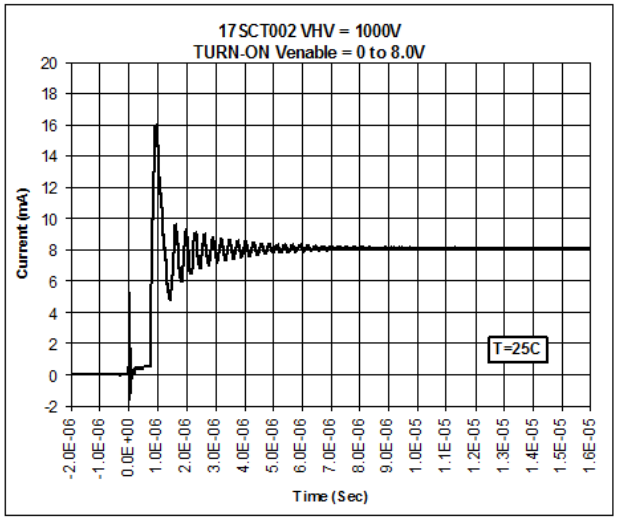


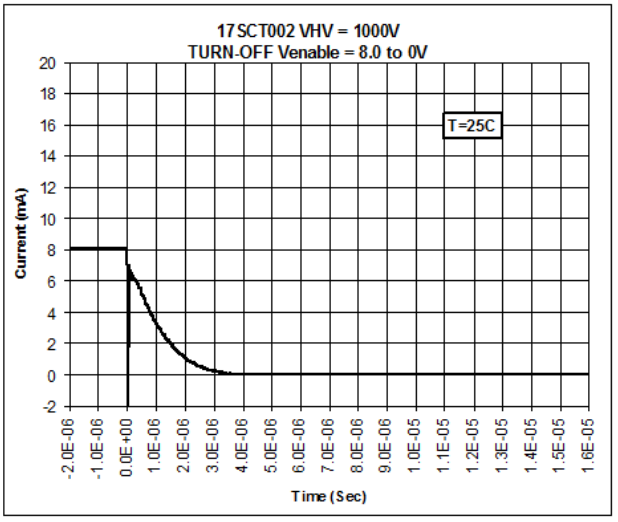


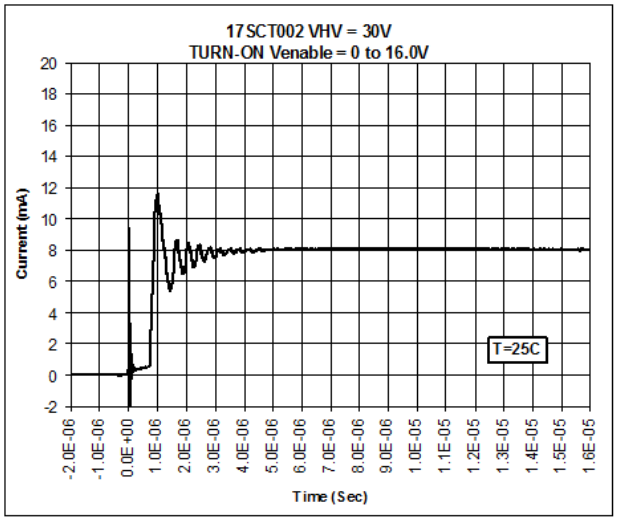


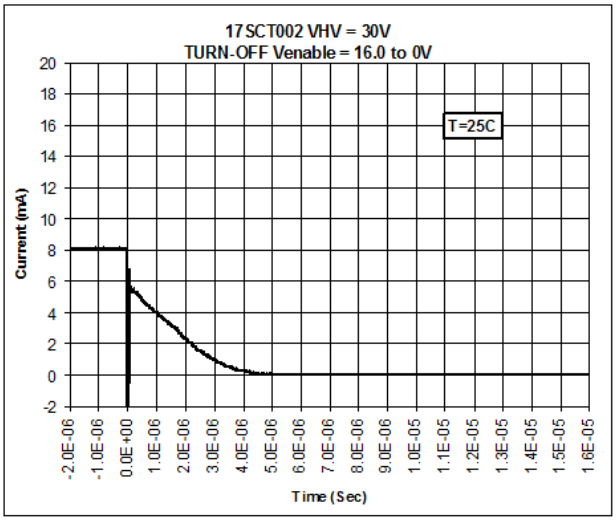


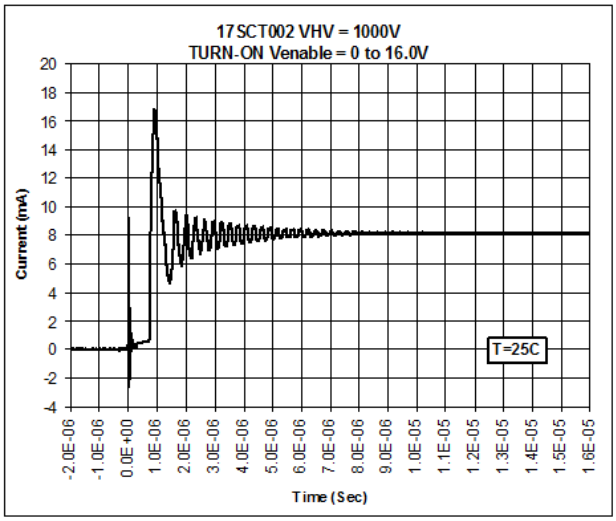


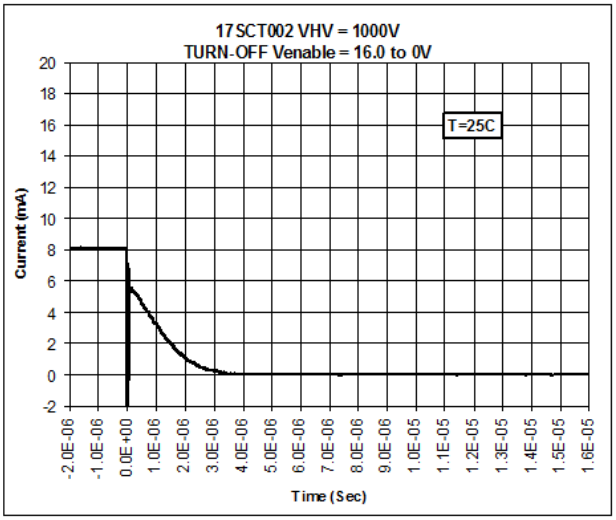






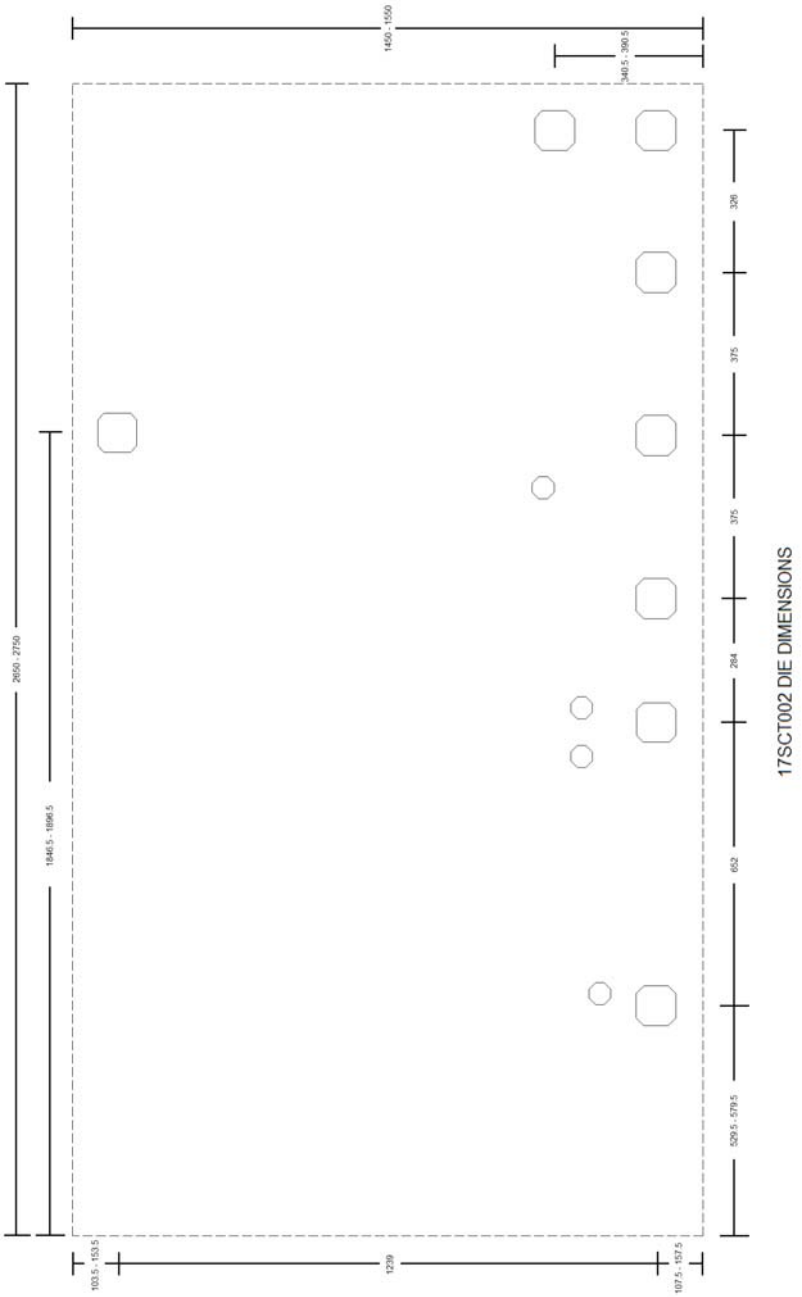






Die Dimensions

PARAMETER		MIN	TYP	MAX	UNIT
Y_{SIZE}	Long Side Dimensions	2650	2700	2750	µm
X_{SIZE}	Short Side Dimensions	1450	1500	1550	µm
Z_{SIZE}	Die Thickness	260	285	310	µm



Visual inspection

PARAMETER	Lot Sampled	Sample Size	Fails Allowed	UNIT
100% Visual Inspection per MIL STD 883H Method 2010 Condition B.	ALL	100%	n/a	n/a

Product qualification tests

PARAMETER	Lot Sampled	Sample Size	Fails Allowed	UNIT
Static burn-in 504hrs @ V_{HV}=1000V; MIL STD 883 method 1015	3	22	0	n/a
Physical dimensions	3	11	0	n/a
Wire Bond Evaluation (Gold Ball Bond) per MIL STD 883 method 2011	3	20	1	n/a

Lot acceptance tests

PARAMETER	Lot Sampled	Sample Size	Fails Allowed	UNIT
Static burn-in 168hrs @ V_{HV}=1000V; MIL STD 883 method 1015	each	22	0	n/a
Physical dimensions	each	11	0	n/a
Wire Bond Evaluation (Gold Ball Bond) per MIL STD 883 method 2011	each	20	1	n/a

Product qualification tests are performed on 3 lots while a Lot Acceptance Test (LAT) is performed on each “diffusion lot”. LAT is considered complete if the lot was used for product qualification.

All samples used for qualification and LAT burn-in test are assembled in a open cavity ceramic DIL package with a dielectric silicone gel filling the cavity. Tthe chip is mounted to provide isolation between the wirebonds and the substrate and to eliminate surface conduction and polarization as possible means of unwanted failure.

Application notes

To make best use of the 17SCT002, the chip should be molded before high voltage is applied to it. This can either be done with a standard mold compound or with silicone gel. Care should be taken when selecting a encapsulant to ensure proper dielectric strength and resistance. We recommend that the dielectric strength of the dielectric used be greater than 10kV/mm at a thickness of 50um.

Care should also be taken to properly isolate the chips substrate which is biased at about half V_{HV}. In no circumstance should the chip be mounted over layers providing less than 1kV of dielectric isolation. It is also strongly recommended to use non-conducting epoxy for attaching the chip.

Ball bonding should be used for attaching conductors to the chip's pad. Wedge bonding is not recommended because of the shorter distance between the wirebond and the chip's edge, increasing the risk of arcing. When using ball bonding the wire should extend vertically for at least 150um before going horizontal toward the substrate or package pad.